REMARKS

The foregoing amendments and the following remarks are responsive to the September 24, 2003 Final Office Action and were initially submitted to the Examiner on December 23, 2003. Claim 4 remains as originally filed, claims 1, 2, and 5-10 are cancelled without prejudice, and claim 3 is amended. In an Advisory Action dated January 26, 2004, the Examiner states that the proposed amendments would not be entered because the amendment to independent claim 3 requires further searching and/or consideration. Thus, claims 3, 4, and 11 are presented again in this submission for further consideration. Please enter the amendments and reconsider the claims in view of the following remarks.

Notice Regarding Change of Attorney Reference Number

Please note that the Attorney Reference Number for the present application has been changed from "IMEC169.001APC" to --FILLF6.001AUS--.

Response to Notice of Draftsperson's Patent Drawing Review

In the September 24, 2003 Office Action, the Draftsperson objected to the margins of Figure 4 and the lines, numbers, and letters of Figures 1-8. Six Replacement Pages were previously filed on December 29, 2003 which provided corrected drawings corresponding to Figures 1-8. In the January 26, 2004 Advisory Action, the Examiner stated that these drawing corrections were approved.

Response to Rejection of Claims 3, 4, 10, and 11 Under 35 U.S.C. § 103(a)

In the September 24, 2003 Office Action, the Examiner rejects claims 3, 4, 10, and 11 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,001,359 to Hashimoto et al. ("the '359 reference") in view of U.S. Patent No. 5,311,320 to Hashimoto ("the '320 reference").

Claim 3

As described herein, Applicants have amended claim 3 to include the limitation that "said column amplifying elements (A_j) and the common output amplifier (D) are connected by a single bus." Thus, amended claim 3 makes clear that there is only one single common output bus, and that all column amplifying elements (A_j) are connected via that one single common output bus to the common output amplifier (D). Support for this wording can be found in Figure 2 of the present application, where a single common output bus between the column amplifying elements (A_j) and the common output amplifier (D) is shown.

Applicants submit that amended claim 3 is patentably distinguished over the '359 reference in view of the '320 reference. In the '359 reference, an image sensor is described as comprising an array of columns and rows of pixels (Figure 4 of the '359 reference). All the pixels of one column of the array are connected to one common pixel output line, as can be seen in Figure 4. Such common pixel output line has two memory elements (Ct1 and Ct2) and a column amplifying element (Q). Each common pixel output line is divided through switches (Qb1 and Qb2) into two parallel circuits before the column amplifying element (Q), the parallel circuits have said memory element (Ct1 and Ct2). The two parallel circuits are connected through a switch (Qt1 and Qt2) with the same input of the column amplifying element (Q).

The '359 reference does not disclose that there is a common output amplifier to which all of the column amplifying elements are connected. Furthermore, the '359 reference does not disclose that the column amplifying elements and the common output amplifier are connected by a single bus.

Instead, in the '359 reference, one column is connected to two busses. Whether these two busses each have a separate output amplifier, as in Figure 3A of the '320 reference, or whether these two busses have a common output amplifier, as in Figure 3B of the '320 reference, does not make any difference; two busses remain, each having its own, and often different, characteristics.

If two busses are present, measures should be taken in order to overcome non-uniformity of the busses, as is also explained with respect to Figure 1a of the present application, where a crossbar switch S2 is provided to average out errors due to the differences between the busses.

This necessity for special measures is overcome in embodiments of the present invention by having a single bus between all the columns and the common output amplifier. An image sensor with a single output bus between the column amplifying elements and the common output amplifier is more accurate than a prior art image sensor having at least two output busses between the column amplifying elements and the common output amplifier.

Furthermore, having a single bus between each of the columns and the common output amplifier has the advantage that less output lines are needed. This is a positive effect, as these output lines have significant dimensions as they run over the whole width of the array of pixels. Reducing the number of output lines reduces the space needed on a chip containing a pixel according to embodiments of the present invention, and thus reduces dimensions of the image sensor.

In view of the above remarks, Applicants submit that amended claim 3 is patentably distinguished over the '359 reference in view of the '320 reference.

Claims 4, 10, and 11

As described herein, Applicants have cancelled Claim 10 without prejudice. Claims 4 and 11 each depend from amended claim 3, so claims 4 and 11 each includes all the limitations of amended claim 3, as well as other limitations of particular utility. Therefore, Applicants submit that claims 4 and 11 are also patentably distinguished over the '359 reference in view of the '320 reference.

Summary

For the foregoing reasons, Applicants submit that claims 3, 4, and 11 are in condition for allowance, and Applicants respectfully request such action.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

Dated: 2/18/04 By: _____

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